

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,903,446 B2
APPLICATION NO. : 10/045766
DATED : June 7, 2005
INVENTOR(S) : Ralph C. Tuttle et al.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 8, line 35, delete the following claims 1-12 and insert the following:

That which is claimed is:

1. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n , where n is at least 2.
2. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n where n is at least 2;
a second metal layer on portions but not all of said surface of said semiconductor material;
said second metal layer forming a pattern different from said first metal layer pattern;
said second pattern having rotational symmetry of C_n where n is at least 2; and wherein
each of said first and second patterns forms an X pattern.
3. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n , where n is at least 2;
a second metal layer on portions but not all of said surface of said semiconductor material;
said second metal layer forming a pattern different from said first metal layer pattern;
said second pattern having rotational symmetry of C_n where n is at least 2;
wherein each of said first and second patterns forms an X pattern; and
wherein each X pattern further comprises a tab portion perpendicular to at least one of the arms of said X pattern.
4. A labeled semiconductor material according to claim 1 wherein said metal layer is selected from the group consisting of nickel, titanium, gold, platinum, vanadium, aluminum, alloys thereof and layered combinations thereof.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

5. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern;
and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers.

6. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern;
and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers;
wherein said substrate and said epitaxial layer comprise a semiconductor device.

7. A semiconductor structure according to claim 6 wherein said device is selected from the group consisting of junction diodes, bipolar transistors, thyristors, MESFETS, JFETS, MOSFETs and photodetectors.

8. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern;
and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers;
wherein said substrate and said epitaxial layer comprise a semiconductor device; and
wherein said metal layers form an ohmic contact to said device.

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9. A semiconductor structure according to claim 8 wherein said substrate and said epitaxial layer are silicon carbide and said metal layers are selected from the group consisting of nickel, titanium, gold, alloys thereof, and layered combinations thereof.

10. A semiconductor device according to claim 8 wherein said device comprises a light emitting diode or laser diode that includes a p-n junction, and with said ohmic contact comprising a layer of nickel on said substrate and a layer selected from the group consisting of titanium-gold alloys and titanium-platinum-gold alloys on said nickel layer.

11. A semiconductor wafer comprising:
a silicon carbide substrate and at least one silicon carbide epitaxial layer;
respective primary and secondary orthogonal flats;
respective front and back planar faces;
a plurality of devices on said wafer;
each said device having a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and
each said device having a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern.

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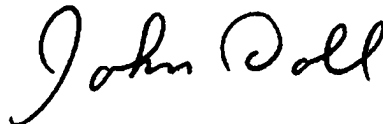
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12. A semiconductor wafer according to Claim 11 wherein:
said devices comprise light emitting diodes or laser diodes that include a p-n junction;
and
said metal layers comprise a layer of nickel on said substrate and a layer of a
titanium- gold alloy on said nickel layer that form respective ohmic contacts to said
devices.

Signed and Sealed this

Third Day of February, 2009



JOHN DOLL

Acting Director of the United States Patent and Trademark Office